Real Time (>1GSS) Digital Signal Processing System Architecture

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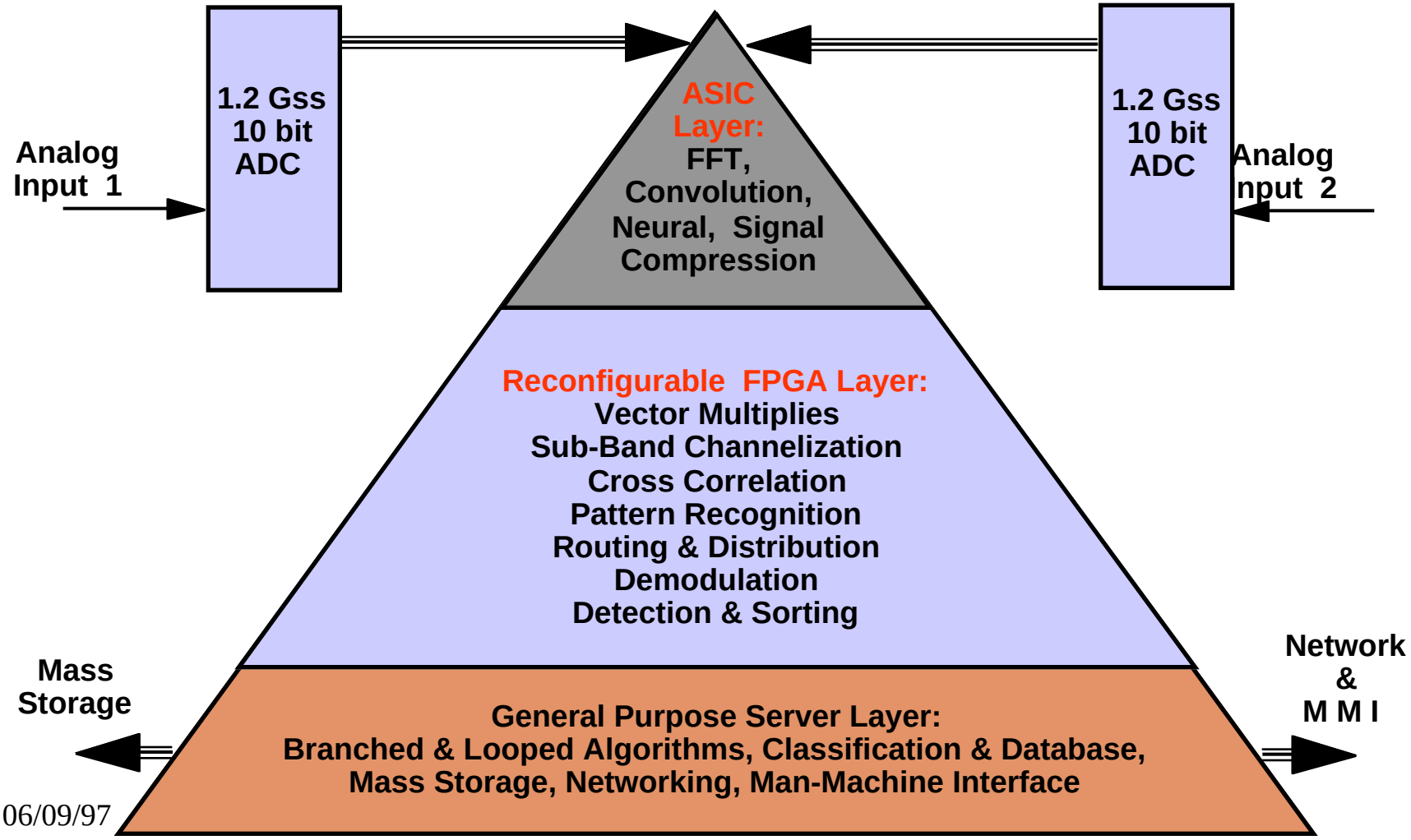
General System Requirements

- Process modern signals, with pre-D methods, as they are generated by the sensor.
- Solve a multitude of complex RT problems without complete system redesign for each problem.
- Integrate many different COTS tools in an open standard for cost efficient supercomputing.
- Support TeraOps processing loads for filtering, FFT, cross correlation and recognition at > 1GSS rates.

Reconfigurable Signal Processing Architecture

- Reconfigurable, no new system designs to solve most new problems.
- Scaleable, allowing fast innovation incorporation.
- COTS components when possible, custom when necessitated by mission requirements.

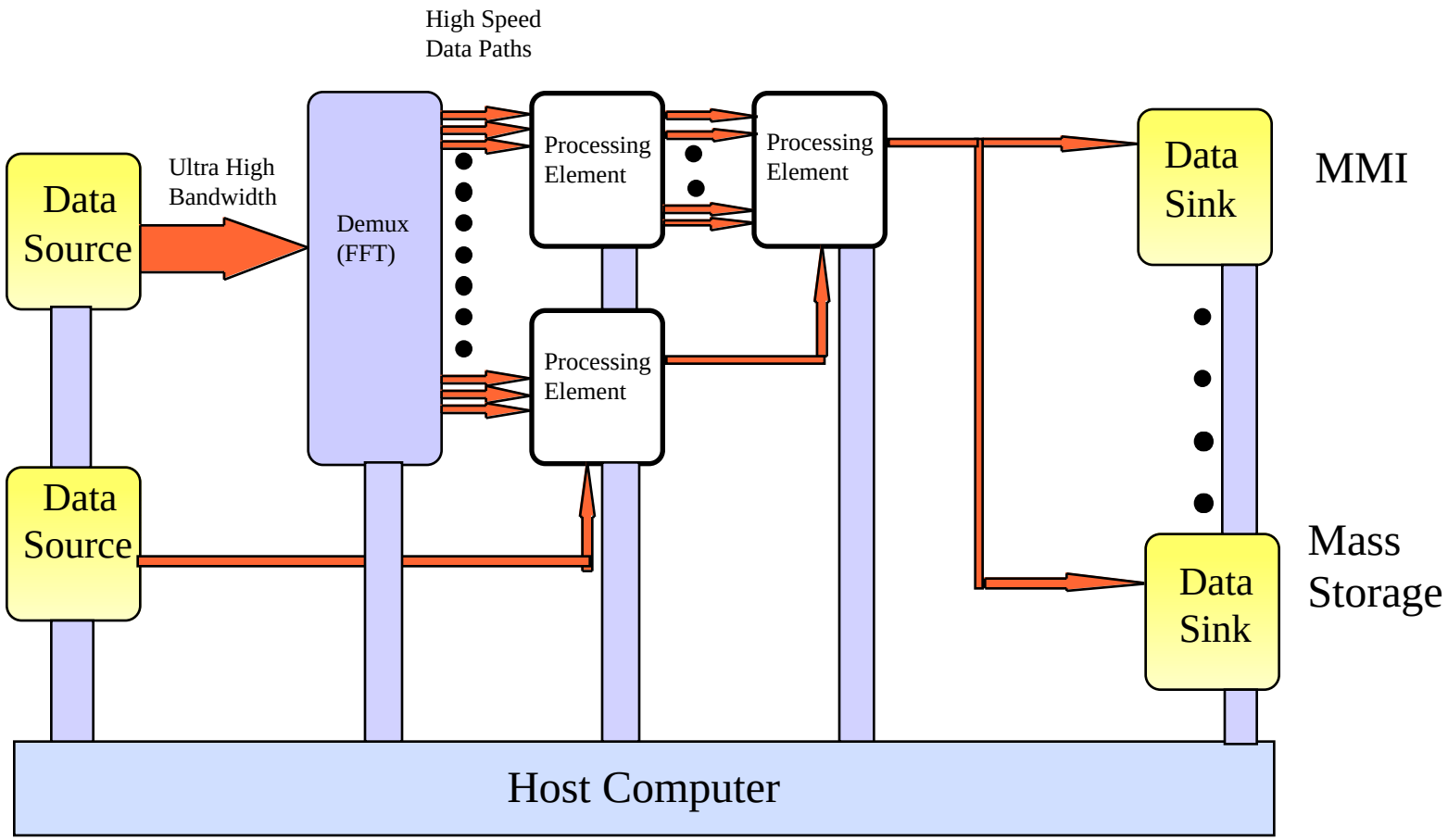
500 MHz Signal Processing via Reconfigurable Computing



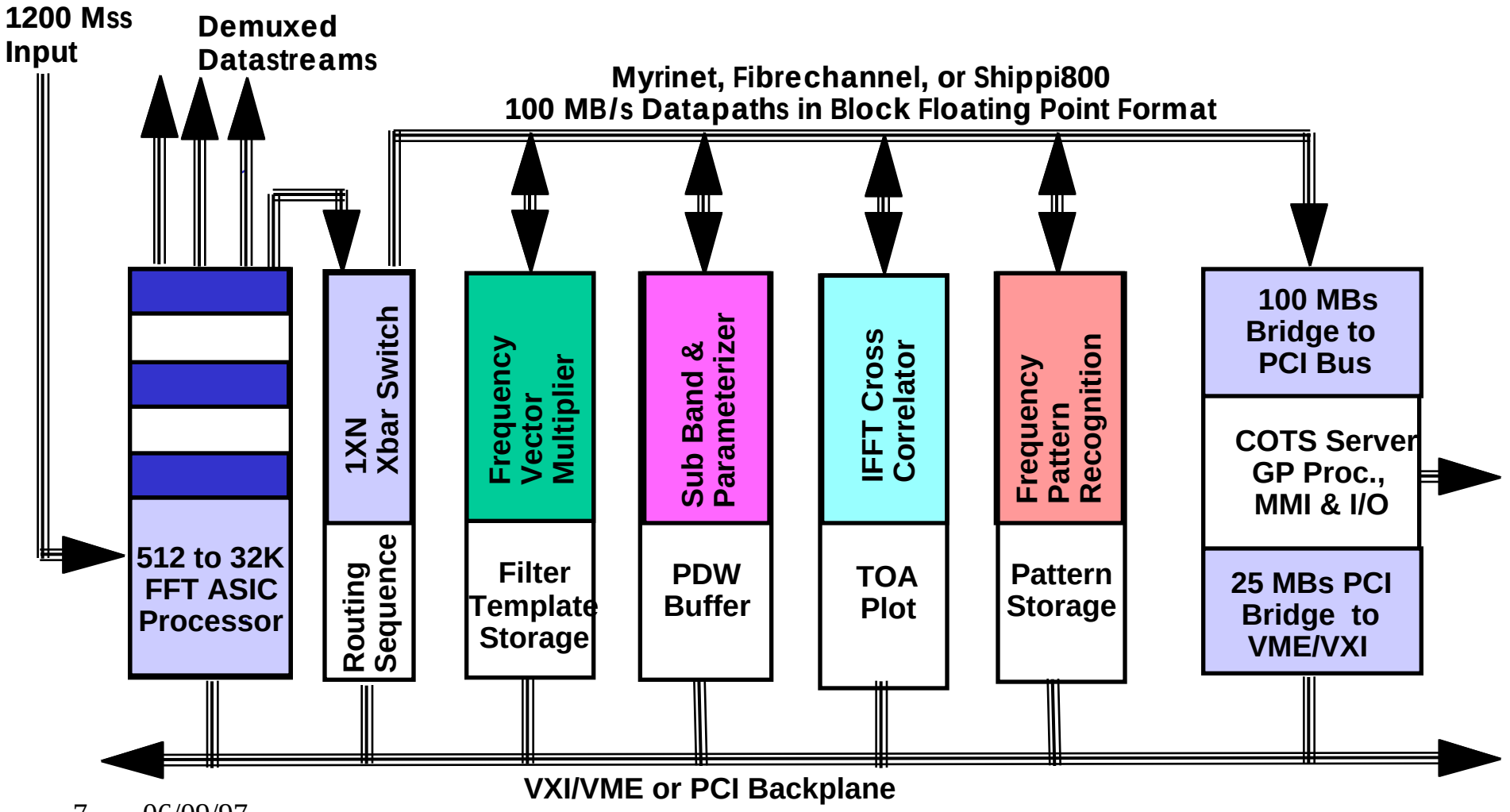
Reconfigurable Processor Key Components

- System Controller (General Purpose workstation)
- Industrial Computer Bus for Control & Status
- High Speed Dedicated Digital Data Paths and Crossbar Switches
- Data Source & Sink Nodes
- Computational Nodes

Reconfigurable Computing Architectures



Modular, Scaleable 100 Mss Base Architecture



System Controller (Host)

TASKS

- Configuration, Initialization & Program Download
- Man Machine Interface (MMI)
- Results Export & Archive
- Branched & Looped Algorithms
- I/O Routing
- Remote Login
- Status Monitor

Contenders (Workstations and Embedded Controllers)

- Alpha
- Wintel P6
- Sparc
- SGI

Control / Status Bus

- Requirements:
  - Power
  - Cooling
  - Board Real Estate
  - COTS * (+ Quality Software from Vendor components)
  - EMI Shielding
  - Speed
  - Legacy Compatibility
- Contenders
  - VME (6U)
  - VME (9U)
  - VXI
  - PCI
  - CompactPCI

High Speed Digital Data Paths & Crossbars to Connect System Nodes

- Requirements
  - Parallel Copper & Serial Optical
  - >100 Mbytes / sec capacity
  - 5 cm - 1 km link distance options
  - COTS bus interfaces & interface chips with vendor SW drivers
  - COTS crossbar switches
  - Low Power, small transceiver footprint (mezzanine size)
- Contenders
  - HIPPI 800, 1600, 6400
  - HP Glink
  - Fibre Channel
  - Raceway & FPDP
  - SkyChannel
  - FDDI
  - ATM (SONET OC12)
  - Alink
  - SCI
  - MyriNet

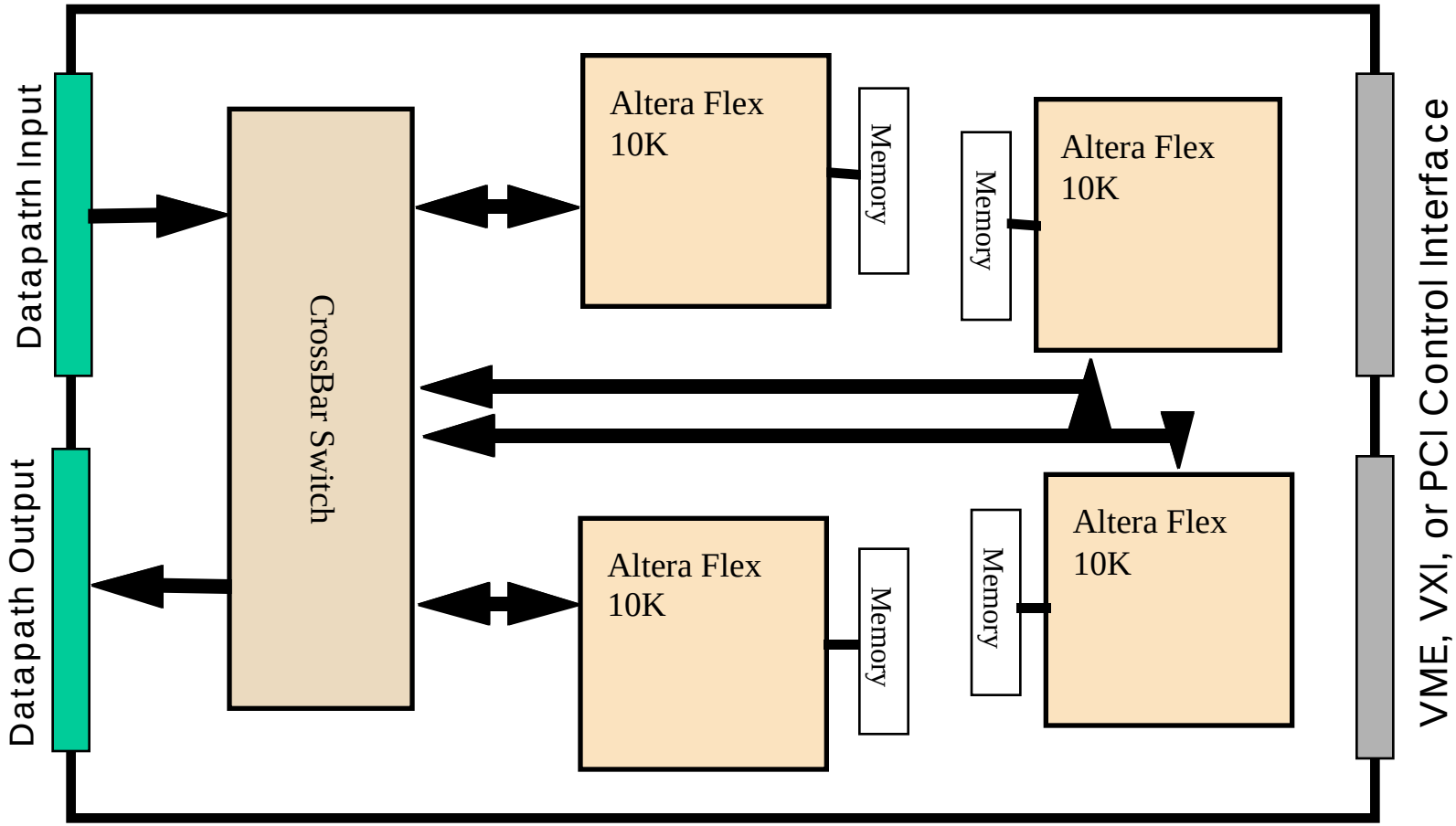
System Nodes : Data Sources and Sinks

- Source Nodes
  - Digital Receivers
  - Digitizers & Video Cameras
  - General Purpose CPU & Custom Signal Processors
- Sink Nodes
  - Mass Storage e.g.. 1 TB tape cartridge, recorders
  - Displays, Long Haul Export
  - Larger System Servers

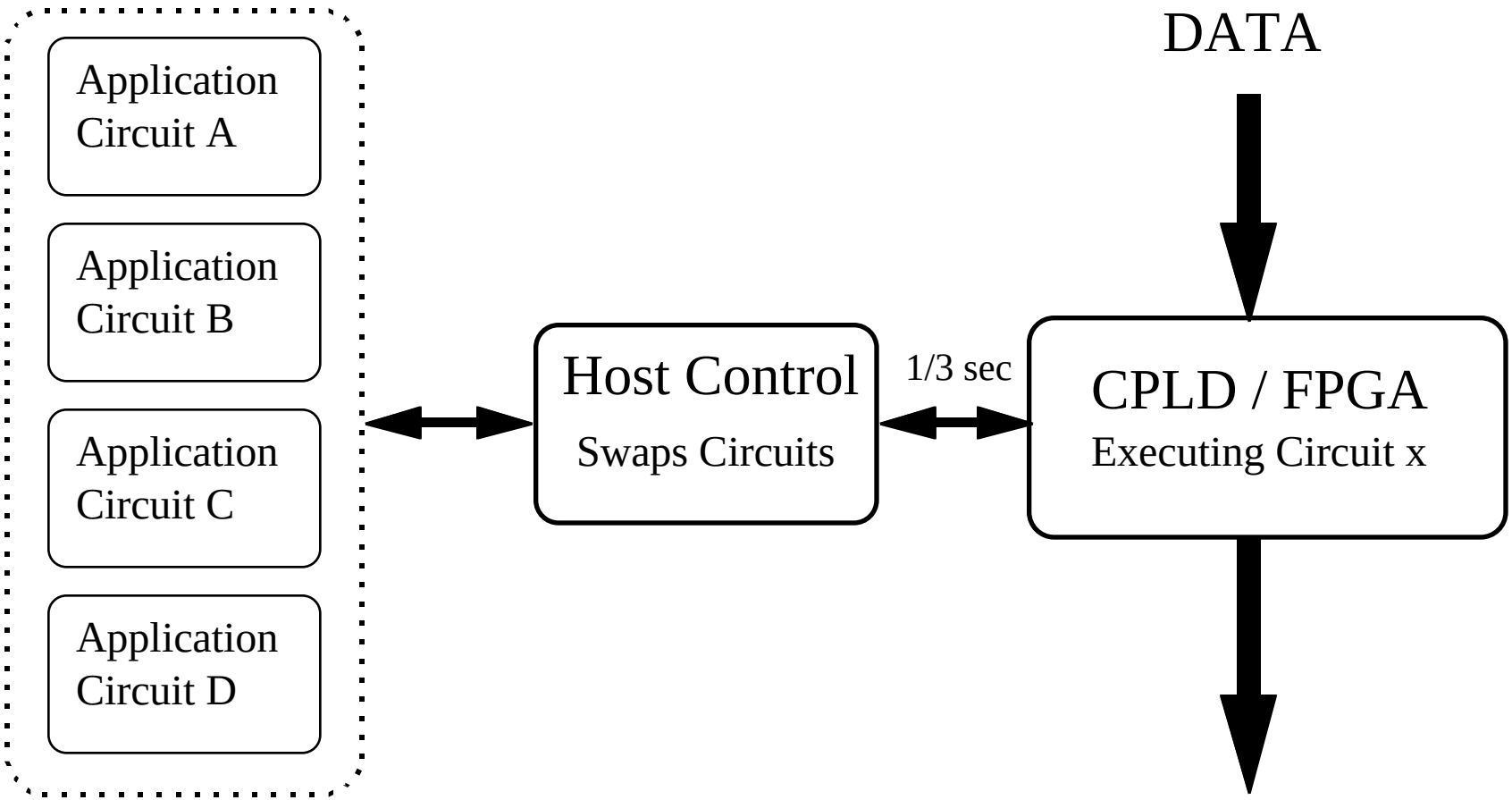
Computation System Nodes

- ASICs
  - 2 - 100x speed and density advantage over FPGAs
  - Expensive to design & build
  - Single task, not reprogrammable
  - Mux/Demux processes (FFT)
- FPGAs and CPLDs
  - 2 - 100x speed and density advantage over DSPs
  - Inexpensive to design & build (Gate Level Design)
  - In circuit reprogrammable
  - Integer, small word signal processing for parallel pipelined algorithms
- DSPs & general purpose processors
  - Comparatively Slow per CPU
  - Inexpensive (software)
  - Extremely flexible and programmable (C/C++)
  - Floating point, larger words, complex algorithms

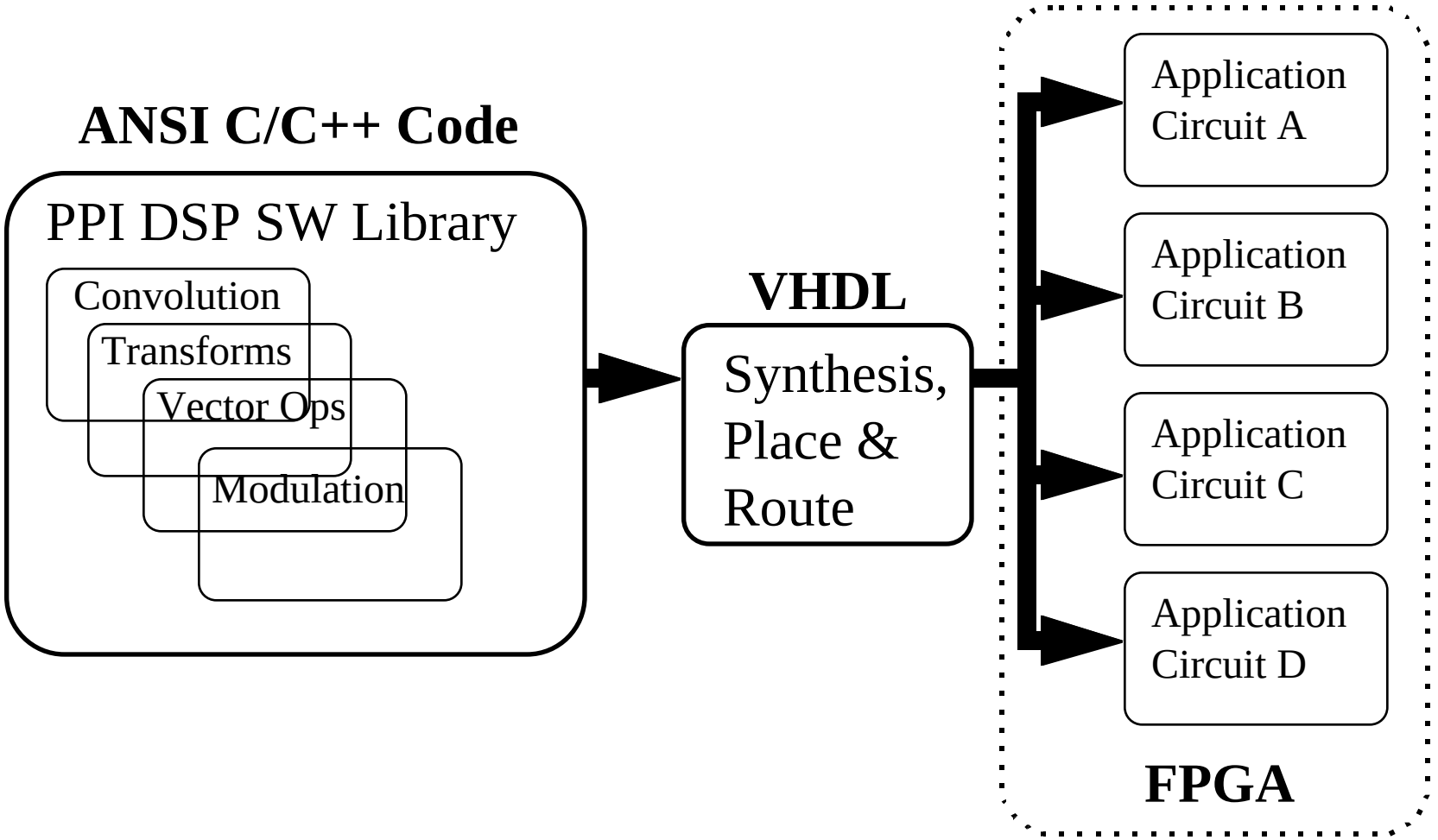
Prototype Configurable Computer



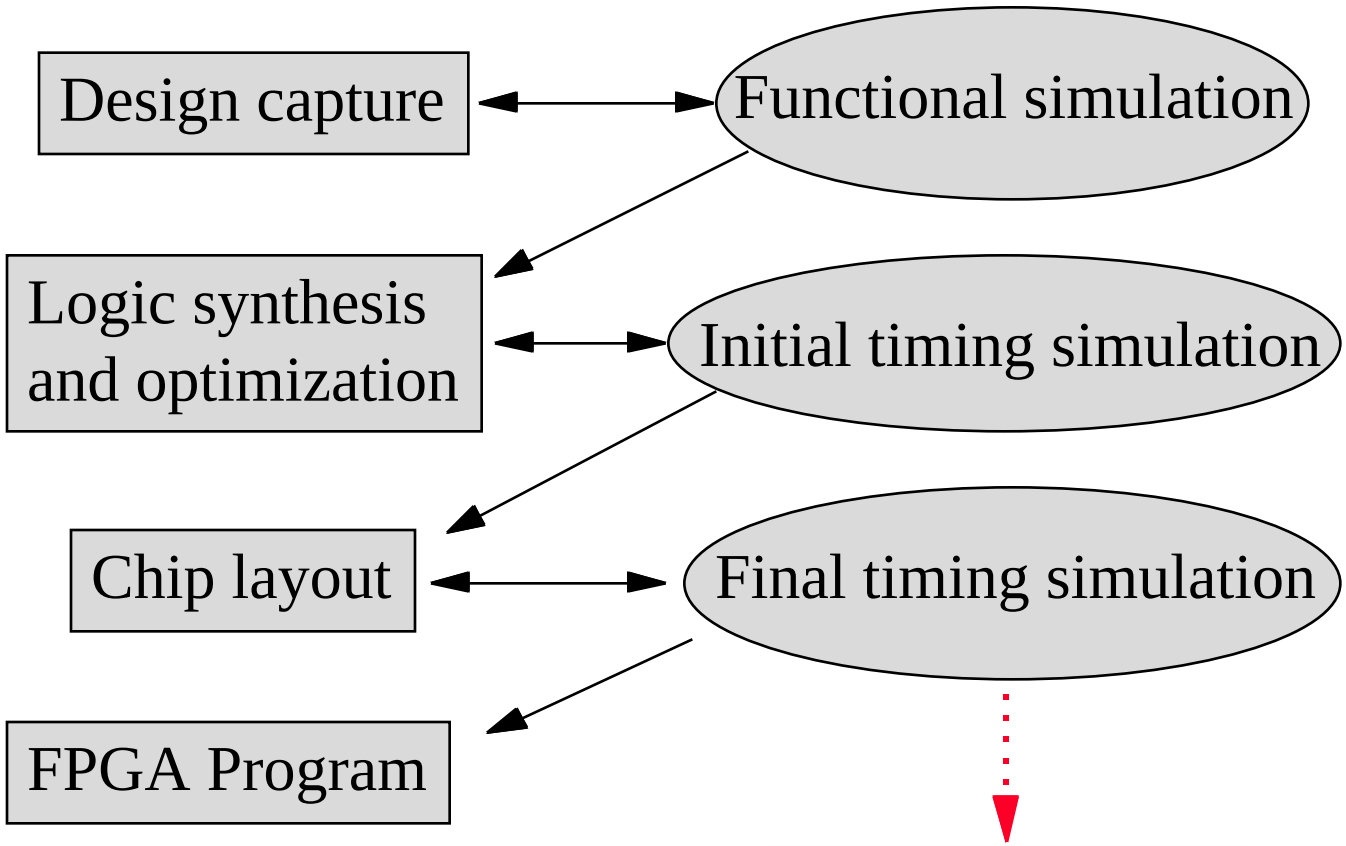
Reconfigurable Computer Operations



Reconfigurable Computing Programming Sequence

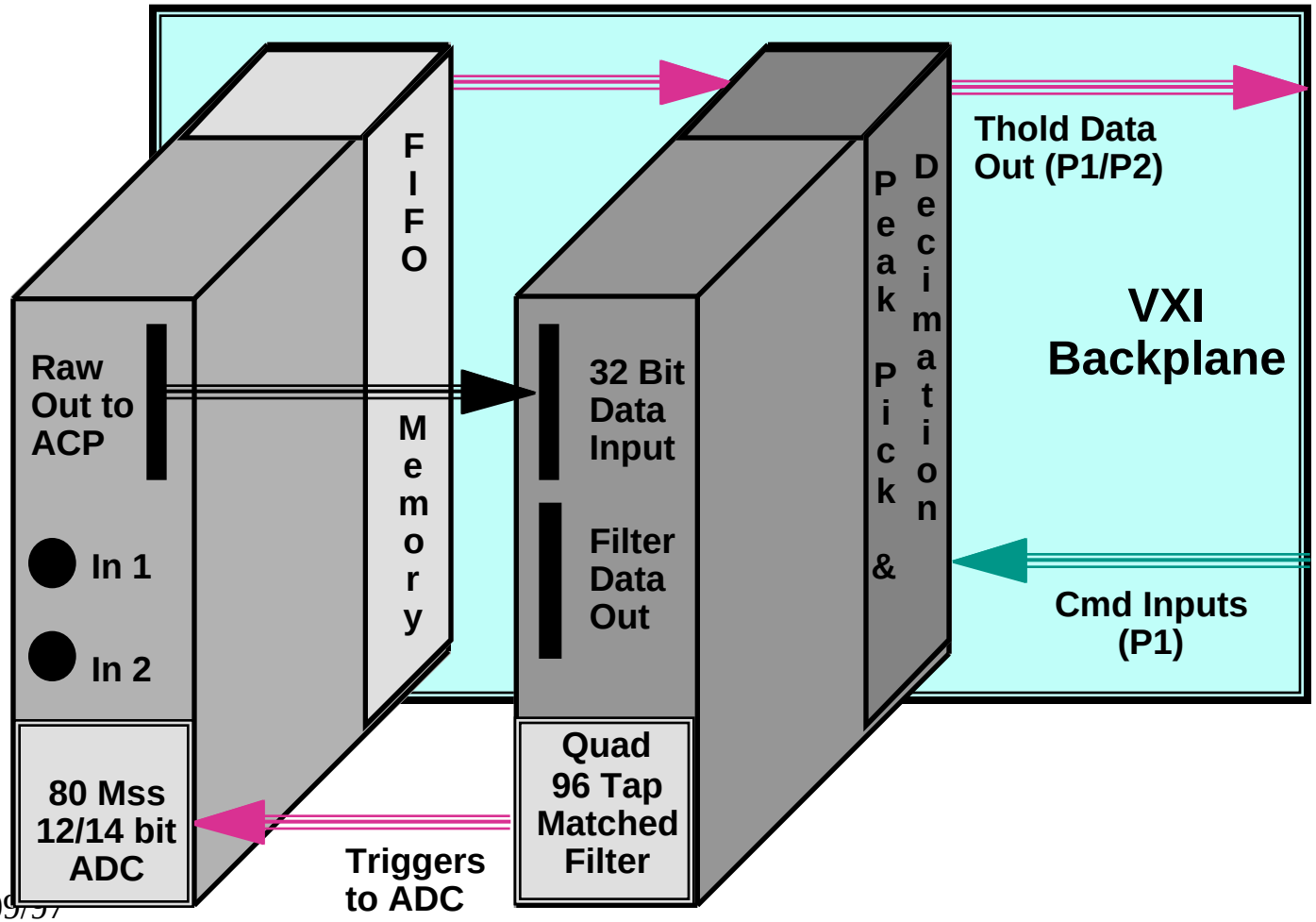


VHDL Design Process

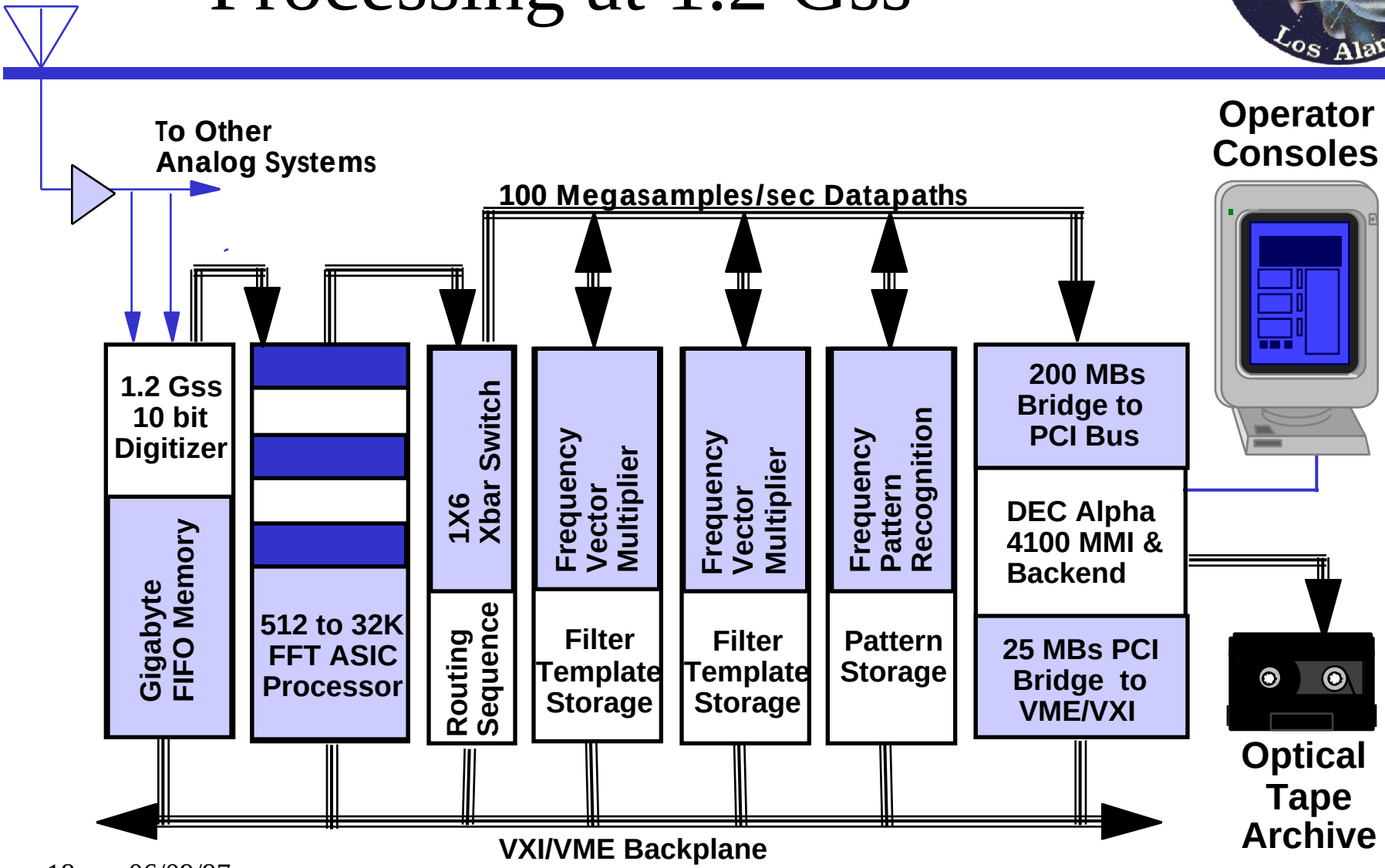


VHDL = VHSIC Hardware Design Language
VHSIC = Very High Speed Integrated Circuit

First Testbed: VXI ADC & Convolutional Detector



Coherent, PreDetection Processing at 1.2 Gss



Why is RCC A Good Investment for LANL & Sponsors?

- RCC is a critical technology: cost-effectively processing more information, without adding ASIC or supercomputer CPU costs
- RCC enables LANL and Sponsor programs:
  - RF smart trigger systems (Aldebaran)
  - Wideband continuous processing (Aldebaran)
  - IR video processing (Caliope)
  - Laser range correction and integration (Caliope)
  - Others: MTI image processing, ATR & compression